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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/889,798	07/20/2001	Hiroshi Hatae	520.40265X00	8803

24956 7590 03/24/2005

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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 03/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

HC

Office Action Summary	Application No.	Applicant(s)	
	09/889,798	HATAE ET AL.	
	Examiner	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 November 2004 and 10 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10 February 2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. New claims 21-24 have been considered. Claims 1-20 have been cancelled as per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as received in 22 November 2004 and IDFS as received on 10 February 2005.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claim 23 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 23 recites the limitation "wherein said arithmetic and logic unit is provided from said data" and "operates said arithmetic operations using said data". After perusing the specification, these limitation could not be found within the written description.

5. Claim 23 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 23 recites the limitation

"wherein said arithmetic and logic unit is provided from said data" and no where in the written description is an explanation of how the ALU is provided, i.e. made available or supplied, by the data and how the ALU can use the same data that is furnishing the ALU for use.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 23 is recites the limitations "wherein said arithmetic and logic unit is provided from said data". There is insufficient antecedent basis for this limitation in the claim.

8. Claim 23 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 23 recites the limitation "which bit width is equal to said second bus", but it is unclear which element, the ALU or the data, has a bit width equal to the second bus. Also, the limitation "operates said arithmetic operations using said data" is unclear as to whether the ALU or arithmetic operations operates using the data, since the ALU is supplied by the data.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 21-24 are rejected under 35 U.S.C. 102(b) as being taught by Nguyen et al., U.S. Patent Number 5,838,984 (herein referred to as Nguyen).

11. Referring to claim 21, Nguyen has taught a data processor comprising:

a. A central processing unit (CPU) which fetches an instruction, decodes said instruction and executes said instruction (Nguyen column 3, lines 61-63; column 4, lines 34-42; and Figure 1);

b. A first data bus coupled to said CPU (Nguyen column 3, line 59 to column 4, line 3 and Figure 1). In regards to Nguyen, Figure 1 shows a 32-bit bus connecting the master processor 110 to caches 162 and 164.

c. An arithmetic and logic unit which operates to perform an arithmetic operation (Nguyen column 4, lines 42-49; column 7, lines 9-13; column 9, lines 1-3; Figure 1; and Figure 2);

d. A memory unit which stores results of said arithmetic operation (Nguyen column 4, lines 15-25; column 7, lines 9-13; column 10, lines 5-05; Figure 1; and Figure 2);

e. A second data bus coupled to said arithmetic and logic unit and said memory unit (Nguyen column 3, line 59 to column 4, line 3 and Figure 1). In regards to Nguyen, Figure 1 shows a 288-bit bus connecting the vector processor 120 to caches 192 and 194.

f. An address bus coupled to said central processing unit, said arithmetic and logic unit and said memory unit (Nguyen column 3, line 63 to column 4, line 3; column 4; column 4, lines 15-33; and Figure 1). In regards to Nguyen, there are buses connecting the processors to cache subsystem 130 and the DMA controller 154 and memory controller 158. There must be an address bus connecting the

processors, cache subsystem, and other devices that need to know the address from one of the processors to read/write data.

g. Wherein a bit width of said second data bus is wider than a bit width of said first data bus (Nguyen column 3, line 59 to column 4, line 3 and Figure 1). In regards to Nguyen, the first bus is 32-bits wide and the second bus is 288-bits wide.

h. Wherein said CPU provides a plurality of control signals to said arithmetic and logic unit in response to a result of decoding a first instruction to control said arithmetic and logic unit (Nguyen column 6, lines 18-39 and Figure 1), and

i. Wherein said arithmetic and logic unit is provided data from said memory unit via said second data bus (Nguyen column 3, line 59 to column 4, line 3 and Figure 1), and is capable of operating a plurality of said arithmetic operations using said data according to said control signals related to said first instruction (Nguyen column 4, lines 44-46; column 6, lines 18-39 and Figure 1).

12. Referring to claim 22, Nguyen has taught wherein said arithmetic and logic unit accesses said memory unit according to an address provided from said CPU (Nguyen column 4, lines 22-23).

13. Referring to claim 23, Nguyen has taught wherein said arithmetic and logic unit is provided from said data, which bit width is equal to said second data bus, according to an address from said CPU, and operates said arithmetic operations using said data (Nguyen column 4, line 63 to column 5, line 2; column 6, lines 18-33; Figure 1; and Figure 2).

14. Referring to claim 24, Nguyen has taught a data processing unit comprising:

a. A central processing unit (CPU) which decodes and executes instructions (Nguyen column 3, lines 61-63; column 4, lines 34-42; and Figure 1);

b. A first data bus coupled to said CPU, and having a first bit width (Nguyen column 3, line 59 to column 4, line 3 and Figure 1). In regards to Nguyen, Figure 1 shows a 32-bit bus connecting the master processor 110 to caches 162 and 164.

c. A single instruction multiple data (SIMD) type arithmetic and logic unit controlled by said CPU (Nguyen column 4, lines 42-49; column 7, lines 9-13; column 9, lines 1-3; Figure 1; and Figure 2);

d. A memory accessed by said SIMD type arithmetic and logic unit as a work area (Nguyen column 4, lines 15-25; column 7, lines 9-13; column 10, lines 5-05; Figure 1; and Figure 2);

e. A second data bus coupled to said SIMD type arithmetic and logic unit and said memory, and having a second bit width (Nguyen column 3, line 59 to column 4, line 3 and Figure 1). In regards to Nguyen, Figure 1 shows a 288-bit bus connecting the vector processor 120 to caches 192 and 194.

f. An address bus coupled to said CPU, said SIMD type arithmetic and logic unit and said memory (Nguyen column 3, line 63 to column 4, line 3; column 4; column 4, lines 15-33; and Figure 1). In regards to Nguyen, there are buses connecting the processors to cache subsystem 130 and the DMA controller 154 and memory controller 158. There must be an address bus connecting the processors, cache subsystem, and other devices that need to know the address from one of the processors to read/write data.

g. Wherein said second bit width is wider than said first bit width (Nguyen column 3, line 59 to column 4, line 3 and Figure 1). In regards to Nguyen, the first bus is 32-bits wide and the second bus is 288-bits wide.

h. Wherein said CPU causes said SIMD type arithmetic and logic unit to operate to perform an arithmetic operation according to a result of decoding a predetermined instruction (Nguyen column 6, lines 18-39 and Figure 1),

i. Wherein said CPU is capable of generating an address to access said memory by said SIMD type arithmetic and logic unit, and

j. Wherein in accordance with a result of decoding said predetermined instruction, said SIMD type arithmetic and logic unit accesses said memory based on said address and operates a plurality of arithmetic operations using data by accessing said memory (Nguyen column 4, lines 44-46; column 6, lines 18-39 and Figure 1).

Response to Arguments

15. Applicant's arguments with respect to claims 21-24 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

16. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

17. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

19. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

20. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
18 March 2005

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